Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A voltage regulator apparatus, comprising:
a voltage regulator having a output terminal to provide an output voltage regulated according to a reference voltage;
a first transistor having a first terminal coupled to a positive terminal of a voltage source, a second terminal coupled to a first bias, and a third terminal coupled to the output terminal of the voltage regulator; and
a second transistor having a first terminal coupled to the third terminal of the first transistor, a second terminal coupled to a second bias, and a third terminal coupled to a negative terminal of the voltage source.

[c2] 2. The voltage regulator apparatus as recited in claim 1, wherein the voltage regulator comprises:
an error amplifier having a positive input terminal, a negative input terminal, and an output terminal, wherein the negative input terminal is for receiving the reference voltage;
a third transistor having a first terminal coupled to the positive terminal of the voltage source, a second terminal coupled to the output terminal of the error amplifier,

and a third terminal outputting the regulated output voltage; and

a load circuit used to divide the regulated output voltage, and provide a feedback voltage to the positive terminal of the error amplifier.

[c3] 3. The voltage regulator apparatus as recited in claim 2, wherein the third transistor is a PMOS transistor.

[c4] 4. The voltage regulator apparatus as recited in claim 2, wherein the load circuit comprises:

a first resistor having a first terminal to receive the regulated output voltage, and a second terminal to output the feedback voltage to the positive terminal of the error amplifier; and

a second resistor having a first terminal coupled to the second terminal of the first resistor, and a second terminal coupled to the negative terminal of the voltage source.

[c5] 5. The voltage regulator apparatus as recited in claim 1, wherein the first transistor is an NMOS transistor.

[c6] 6. The voltage regulator apparatus as recited in claim 1, wherein the second transistor is a PMOS transistor.

[c7] 7. The voltage regulator apparatus as recited in claim 1, wherein the first bias is defined for the first transistor

operating in a sub-threshold region.

[c8] 8. The voltage regulator apparatus as recited in claim 1, wherein the second bias is defined for the second transistor operating in a sub-threshold region.